CLAIMS

1. A phase lock loop circuit for a radio frequency transmit and receive apparatus, the circuit comprising:

a first voltage controlled oscillator which is operable to produce a first reference frequency signal,

a second voltage controlled oscillator which is operable to produce a second reference frequency signal,

a switchable set of dividers, connected to receive the first and second reference frequency signals, and operable to produce a set of output reference frequency signals therefrom, a first subset of the set of output reference frequencies being derived from the first reference frequency, and a second subset of the set of output reference frequencies being derived from the second reference frequency, and

a VCO control means connected to receive an external reference signal and a feedback signal, and operable to supply a control voltage to the first and second voltage controlled oscillators in dependence upon received external reference and feedback signals, so as to maintain desired first and second reference frequency signals,

wherein the first and second reference frequency signals are not equal in frequency to the output reference frequency signals in the set of output reference frequency signals, and

wherein the set of dividers comprises:

a first divider for selectively receiving the first or second reference frequency signals, and for producing a high band output reference frequency signal for a transmitter,

a second divider for receiving the second reference frequency signal and for producing a low band output reference frequency signal for the transmitter,

a third divider for selectively receiving the first or second reference frequency signals and for producing local oscillator output reference frequency signals for a receiver, and for producing a feedback signal for supply to the VCO control means.

2. A circuit as claimed in claim 1, wherein the set of output reference frequency signals have frequencies corresponding to frequencies required for GSM850, GSM900, DCS1800 and PCS1900 mobile telecommunications standards.

3. A circuit as claimed in claim 1 or 2, wherein the first and second voltage controlled oscillators are selectively controlled by a phase locked loop.

4. A circuit as claimed in any one of the preceding claims, wherein the set of dividers is operable to vary a modulus value thereof, thereby causing the first and second voltage controlled oscillators to be frequency modulated.

5. A circuit as claimed in claim 4, wherein the modulus value has a fixed portion and a time-varying portion.